WHAT IS CLAIMED IS:

1. An image processor comprising:

a storage circuit storing therein image data;

a data input/output circuit controlling input/output of the image data;

an access control circuit controlling access of writing in and reading out the image data to and from said storage circuit;

a refresh circuit controlling refreshing of said storage circuit; and

a memory control circuit comprising an address generation circuit generating an address in said storage circuit to and from which the image data is written in and read out,

said memory control circuit comprising an area adjustment circuit which sets up an additional area adjacent to an area in which the image data is actually stored in a memory space of said storage circuit and storing therein data other than the image data, which adjusts the address generated by said address generation circuit, and which reads out the image data from said storage circuit, including the data in the additional area, in response to the address and a read control signal supplied to said storage circuit.

2. The image processor in accordance with claim 1, wherein said area adjustment circuit sets up the additional area immediately preceding or following the area in which the image data is stored.

3. The image processor in accordance with claim 1, wherein information on a position of the additional area is supplied as setting information included in header information.

4. The image processor in accordance with claim 2, wherein said area adjustment circuit sets a size of the additional

area using information, which is obtained in synchronization with a supplied vertical synchronization signal, as a parameter and reads out the data stored in the additional area in response to a data transfer request.

5. The image processor in accordance with claim 1, wherein said area adjustment circuit obtains information on a base point in the memory space, a row direction width, and a column direction width and outputs the obtained information to said address generation circuit as a parameter.

6. The image processor in accordance with claim 2, wherein said area adjustment circuit obtains information on a base point in the memory space, a row direction width, and a column direction width and outputs the obtained information to said address generation circuit as a parameter.

7. The image processor in accordance with claim 4, wherein said area adjustment circuit obtains information on a base point in the memory space, a row direction width, and a column direction width and outputs the obtained information to said address generation circuit as the parameter.

8. The image processor in accordance with claim 5, wherein said area adjustment circuit supplies the data, which is read out from the additional area, to a predetermined position in a video signal.

9. The image processor in accordance with claim 6, wherein said area adjustment circuit supplies the data, which is read out from the additional area, to a predetermined position in a video signal.

10. The image processor in accordance with claim 7,

wherein said area adjustment circuit supplies the data, which is read out from the additional area, to a predetermined position in a video signal.

11. The image processor in accordance with claim 1, wherein said access control circuit supplies the data other than the image data to said memory circuit.

12. An image processing method comprising the steps of:

setting up, in a storage circuit in which image data is stored, a range of an image area in which the image data is written and a range of an additional area which is adjacent to the image area and in which data other than the image data is written, with information supplied to a memory space of said storage circuit as a parameter;

writing the data other than the image data from external into the additional area in said storage circuit according to a first write control signal;

writing the image data at an address location of the image area in said storage circuit according to a second write control signal; and

reading out the data stored in the additional area and the image data stored in the image area in said storage circuit in response to a first read control signal.

13. The image processing method in accordance with claim 12, wherein said step of reading out the data comprises the steps of:

reading out the data from the additional area in said storage circuit in response to the first read control signal; and

reading out the image data from the image area in said storage circuit in response to a second read control signal.

14. The image processing method in accordance with claim 12, wherein the first write control signal and the read control signal are a transfer enable signal enabling an execution of processing.

15. The image processing method in accordance with claim 12, wherein said step of reading out the data inserts the data read out from the additional area into a predetermined position of a video signal.

add A2